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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,499	09/30/2003	Motoki Kobayashi	FUJI 137	2321

23995 7590 10/19/2005

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,499	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 3 August 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3,5-7,10-13 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yonehara et al. (U.S. Patent 5,530,266).

Yonehara discloses a semiconductor device (Figs. 15G, 38 and 43) that contains a silicon support substrate (61/44) including a groove (84), a first insulation layer (62/45) on top of the supporting substrate, an SOI layer (71/42) formed on top of the first insulation layer, a first element layer on SOI, at least one analog element (target) (transistor, high frequency circuit) (55/56/57/47) formed on the SOI layer and at least one groove (84) formed in the supporting substrate such that a reverse face of the insulation is exposed and being located below a target element (57) whose dielectric loss is to be controlled among the elements, a second insulation layer (60/750) formed on top of first element layer, at least one additional element layer (58/61/62/726) formed on top of second insulation layer and a plurality of bonding pads (on top of 66/67) formed over substrate and the groove is absent below bonding pads.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara in view of Eda et al. (U.S. Patent 5,668,057).

Yonehara discloses all the limitations except for the analog element to be an inductor. Whereas Eda discloses a semiconductor device (Fig. 6) that contains a supporting substrate (1) with analog elements (3-5) are formed thereon where the analog element is an inductor or a transistor. An inductor is used as a passive chip component. (Column 13, lines 25-30) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have that analog element to be an inductor to act as a passive chip component as taught by Eda.

Claims 14-16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara in view of Eda et al.

Yonehara discloses a semiconductor device (Figs. 15G, 38 and 43) that contains a silicon support substrate (61/44) including a groove (84), a first insulation layer (62/45) on top of the supporting substrate, an SOI layer (71/42) formed on top of the first insulation layer, an analog element (57) formed on the SOI layer and at least one groove (84) formed in the supporting substrate such that a reverse face of the insulation

is exposed and being located below a target element (57) whose dielectric loss is to be controlled among the elements, a second insulation layer (60/750) formed on top of first element layer, at least one additional element layer (61/62/726) formed on top of second insulation layer and a plurality of bonding pads (on top of 66/67) formed over substrate and the groove is absent below bonding pads.

Yonehara discloses all the limitations except for the analog element to be an inductor. Whereas Eda discloses a semiconductor device (Fig. 6) that contains a supporting substrate (1) with analog elements (3-5) are formed thereon where the analog element is an inductor or a transistor. An inductor is used as a passive chip component. (Column 13, lines 25-30) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have that analog element to be an inductor to act as a passive chip component as taught by Eda.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. In regards to the dielectric loss as previously stated, the dielectric loss is dependent on the substrate and as stated in the abstract and the specification of the application (Page 4, 1st paragraph) that the dielectric loss is dependent on the substrate and the dielectric loss is achieved for an element anywhere that a groove is located in the substrate under the element. So the target element would have dielectric loss where the groove is since there is not dielectric material under the element. Therefore the rejection stands.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR